# Article information:

Potential and drain current modeling of surrounding gate MOSFET including polysilicon depletion | IEEE Conference Publication | IEEE Xplore  
<https://ieeexplore.ieee.org/document/6467679>

# Article summary:

1. Surrounding gate MOSFET is a promising device structure for future technology nodes due to its enhanced gate control capability, resulting in greater short channel effect immunity and leakage current reduction.

2. Depending on the applied gate voltage, the surrounding gate MOSFET can work at different modes from heavy accumulation to strong inversion regions, and the polysilicon depletion effect cannot be neglected in nanoscale MOSFETs.

3. An analytical surface potential model and a potential-based drain current model are derived to take into account the polysilicon depletion effect and verified using 3D device simulator SenTaurus Device.

# Article rating:

Appears moderately imbalanced: The article provides some useful information, but is missing several important points or pieces of evidence that would be required to present the discussed topics in a balanced and reliable way. You are encouraged to seek a more balanced perspective on the presented issues by exploring the provided research topics and looking at different information sources.

# Article analysis:

该文章主要介绍了围栅MOSFET的潜力和漏极电流建模，包括多晶硅耗尽效应。然而，该文章存在一些偏见和片面报道。

首先，该文章没有提及围栅MOSFET可能存在的风险和缺陷。例如，由于其复杂的结构和制造工艺，围栅MOSFET可能会导致成本增加和可靠性下降。此外，在实际应用中，围栅MOSFET还需要考虑温度、辐射等因素对器件性能的影响。

其次，该文章没有平等地呈现双方观点。它只强调了围栅MOSFET的优点，并未探讨其他类型的晶体管或器件结构的优缺点。这种单方面宣传可能会误导读者对技术发展趋势的理解。

此外，该文章提出了一些主张，但未提供充分证据来支持这些主张。例如，在第一段中提到，“大大增强了门控能力”，但并未说明如何量化这种增强效果或与其他器件结构进行比较。

最后，该文章忽略了一些重要考虑点。例如，在实际应用中，围栅MOSFET需要考虑电源噪声、布局设计等因素对器件性能的影响。此外，该文章未考虑多晶硅耗尽效应对器件寿命和可靠性的影响。

综上所述，该文章存在一些偏见和片面报道，并未全面探讨围栅MOSFET的优缺点和潜在风险。读者需要谨慎评估其内容并结合其他来源进行分析。

# Topics for further research:

* Potential risks and drawbacks of FinFET technology
* Comparison with other transistor structures and devices
* Quantification of the enhanced gate control capability
* Consideration of power supply noise and layout design in practical applications
* Impact of polycrystalline silicon depletion effect on device lifespan and reliability
* Balanced and unbiased reporting on FinFET technology

# Report location:

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