# Article information:

Selective Multiple Capture Test (SMART) XLBIST | IEEE Conference Publication | IEEE Xplore
<https://ieeexplore.ieee.org/document/9854681>

# Article summary:

1. Logic BIST (LBIST) and XLBIST are important techniques for test cost reduction and silicon life-cycle management in complex digital designs.

2. XLBIST addresses the challenge of unknown unload values (Xs) that can corrupt output responses, and it achieves high compression despite supporting any number and density of Xs in the scan-out responses.

3. The hardware architecture of XLBIST includes separate PRPGs for loading care bits and X-tolerance controls, as well as clock selection strategies to optimize coverage and reduce test cost.

# Article rating:

Appears moderately imbalanced: The article provides some useful information, but is missing several important points or pieces of evidence that would be required to present the discussed topics in a balanced and reliable way. You are encouraged to seek a more balanced perspective on the presented issues by exploring the provided research topics and looking at different information sources.

# Article analysis:

对于上述文章，由于只提供了标题和部分摘要，并没有提供完整的内容，因此无法进行详细的批判性分析。但是从摘要中可以看出，该文章主要介绍了一种名为Selective Multiple Capture Test (SMART) XLBIST的逻辑BIST架构，旨在实现测试成本降低和硅片生命周期管理。该架构通过引入ATPG驱动的多重捕获时钟选择来增加XLBIST覆盖率，并在几个大型设计上展示了一致的XLBIST覆盖率改进结果。

然而，由于缺乏完整的文章内容，无法对其潜在偏见及来源、片面报道、无根据的主张、缺失的考虑点、所提出主张的缺失证据、未探索的反驳、宣传内容等进行具体分析。同时，在没有完整信息的情况下也无法判断作者是否注意到可能存在的风险或是否平等地呈现双方观点。

因此，需要获取完整文章内容才能进行更全面和详细的批判性分析。

# Topics for further research:

* Selective Multiple Capture Test (SMART) XLBIST
* Logic BIST architecture
* Test cost reduction
* Silicon lifecycle management
* ATPG-driven multiple capture clock selection
* Consistent XLBIST coverage improvement results

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